Method of Forming a Polycrystalline Silicon Layer

Cross Reference

This application claims the benefit of Korean Patent Application No. 1999-67846, filed on December 31, 1999, under 35 U.S.C. ~~{§ 119}~~[§119], the entirety of which is hereby incorporated by reference.

Background of the invention

Field of the invention

The present invention relates to a method of forming a polycrystalline silicon layer ~~{of}~~ **[for]** a switching element, for example, a thin film transistor (TFT).

Description of Related Art

A thin film transistor (TFT) includes an insulating layer, a passivation film, electrode layers and a semiconductor layer. The insulating layer is ~~{made}~~ **[beneficially comprised]** of SiNx, SiO_2, Al_2O_3 or TaOx. The passivation film is ~~{made}~~ **[beneficially comprised]** of a transparent organic insulating material or **[of]** a transparent inorganic insulating material. The electrode ~~{layer includes}~~ **[layers include]** a gate electrode, a source electrode**[,]** and a drain electrode ~~{and is made}~~**[, and are beneficially comprised]** of a conductive metal such as Al, Cr or Mo. The semiconductor layer acts as a channel region along which charges flow ~~{and is made}~~**[. The semiconductor layer is usually comprised]** of amorphous silicon or polycrystalline silicon.

A process of forming the semiconductor layer using ~~{the}~~ amorphous silicon can be performed at a low temperature of about 350 °C and ~~{thus}~~ is relatively simple. However, since a field effect mobility of ~~{the}~~ **[an]** amorphous silicon layer ~~{is}~~ **[can be]** as low as 2 $cm^2/V \cdot sec$, ~~{thus,}~~ **[the]** switching characteristics of the TFT ~~{and an incorporation characteristics between a driving circuit and the TFT are not so good.}~~

[are not particularly good.]

~~{Meanwhile, the}~~ **[A]** polycrystalline silicon layer ~~{is}~~ **[has a]** much ~~{more excellent in}~~ **[better speed of]** response ~~{speed}~~ than ~~{the}~~ **[an]** amorphous silicon layer. ~~{The}~~ **[A]** polycrystalline silicon layer ~~{has as}~~ **[can have]** a ~~{high}~~ field effect mobility ~~{as about}~~ **[between]** 20 $cm^2/V \cdot sec$ to about 550 $cm^2/V \cdot sec$. ~~{A}~~ **[As the]** switching speed of ~~{the}~~ **[a]** TFT depends on the field effect mobility~~{. That is, a}~~**[, the]** switching speed of ~~{the}~~ **[a TFT having a]** polycrystalline silicon layer is **[about]** 100 times as fast as that of ~~{the}~~ **[a similar TFT having an]** amorphous silicon layer. ~~{This comes from that the }~~**[The higher field effect mobility is a result of the better grains in a]** polycrystalline silicon layer ~~{is more in grain number and is smaller in defect than the}~~ **[as compared to those of an]** amorphous silicon layer.

~~{A method}~~ **[Methods]** of forming ~~{the}~~ polycrystalline silicon ~~{layer includes}~~ **[layers include]** an ~~{eximer}~~ **[excimer]** laser annealing technique, a solid phase crystallization (SPC) technique, and a metal**[-]**induced crystallization (MIC) technique.

~~{The eximer}~~ **[Excimer]** laser annealing ~~{technique is }~~**[is usually]** performed at a low temperature and, thus a low-cost glass substrate ~~{is}~~ **[can be]** used. ~~{The}~~ **[A]** TFT manufactured using the ~~{eximer}~~ **[excimer]** laser annealing technique **[usually]** has a field effect mobility **[of]** more than 100 $cm^2/V \cdot sec$**[,]** and thus ~~{is}~~ **[has]** excellent ~~{in}~~ operating characteristics.

The solid phase crystallization technique is one **[in]** which amorphous silicon is crystallized at a high temperature ~~{of more than}~~**[, usually over]** 600 °C. Since ~~{a}~~ crystallization is performed at a solid phase, a grain ~~{has many}~~ **[can have]** defects such as a micro-twin, a dislocation ~~{and the like, whereupon a grade of a grain is low}~~**[,**

and the like. Grains obtained using solid phase crystallization are usually of a low grade]. In order to compensate for this ~~{problem}~~, a thermal oxidation film ~~{of}~~ **[formed at]** about 1000 °C is **[usually]** used as a gate insulating layer. Therefore, ~~{since}~~ a high-cost material**[,]** such as quartz**[,]** is ~~{used}~~ **[required]** for the substrate~~{, there is}~~**[. This presents]** a problem **[in]** that ~~{a}~~ production ~~{cost is}~~ **[costs are]** high.

~~{The}~~ **[In the]** metal**[-]**induced crystallization technique ~~{is one that a}~~**[,]** crystallization is performed ~~{in such a way that}~~ **[by depositing]** a metal layer ~~{is deposited on the}~~ **[on an]** amorphous silicon layer ~~{and then a heat treatment is performed}~~ **[which is then heat treated]**. The metal layer ~~{serves to lower an}~~ **[lowers the]** enthalpy of the amorphous silicon layer. As a result, ~~{a process}~~ **[crystallization]** is possible at a low temperature of about 500 °C. However, ~~{a}~~ **[the resulting]** surface state and electrical characteristics are not ~~{so good. This technique also causes many defects in grain. }~~**[particularly good, and the resulting grains can have many defects.]**

~~{The}~~ **[A]** polycrystalline silicon layer manufactured using the techniques described above can obtain grains from silicon seeds ~~{while the silicon of a liquid state is cooled at the beginning stage of crystallization. In case that a grain of the silicon }~~**[formed while the silicon, in a liquid state, cools. If a silicon grain]** grows laterally, large-sized grains can be obtained. If ~~{a}~~ **[the]** distance between adjacent silicon seeds is greater than ~~{a}~~ **[the]** maximum silicon growth distance, ~~{the silicon grain that performs a lateral growth centering the silicon seed grows maximally, and then a small-sized grains are created on a region of a liquid state due to a nucleus generated by a super-cooling. However, a}~~ **[a silicon grain grows laterally with the silicon seed at the center of the grain. After the silicon grain grows to its maximum length, nuclei**

generated by super-cooling create many small-sized grains. However, if the] distance between adjacent silicon seeds is ~~{smaller}~~ **[less]** than ~~{a}~~ **[the]** maximum silicon growth distance, ~~{a lateral growth occurs centering a seed, forming grain boundaries, whereby the polycrystalline silicon layer having large-sized grains is formed. As described above, in order to obtain the excellent TFT, the}~~ **[large sized grains that meet at grain boundaries are formed. To obtain a high-quality TFT,**]large-sized grains should **[be]** uniformly ~~{be}~~ arranged while forming ~~{the}~~ grain boundaries.

Figs. 1A ~~{to 1C}~~ **[and 1B]** are plan views illustrating a crystallization process of a polycrystalline silicon layer. ~~{A}~~ **[The]** distance between ~~{the two}~~ adjacent silicon seeds 11 is ~~{smaller}~~ **[less]** than ~~{a}~~ **[the]** maximum grain growth distance~~{, but it}~~**[. It]** is desirable that the silicon seeds 11 are uniformly distributed. The silicon grains 13 ~~{of a liquid state}~~ grow laterally**[,]** centering on the silicon seed 11**[,]** and complete their growth ~~{while}~~ **[after]** forming grain boundaries 15.

Hereinafter, a crystallization process ~~{of the polycrystalline silicon layer}~~ using the ~~{eximer}~~ **[excimer]** laser annealing technique according to a conventional art is explained in **[more]** detail.

Fig. 2 is a perspective view illustrating a configuration of ~~{a}~~ polycrystalline silicon crystallization equipment using the ~~{eximer}~~ **[excimer]** laser annealing technique. The equipment includes a laser beam device (not shown), a mask 33, and a projection lens 35. The projection lens 35 is arranged over a substrate 31, and the mask 33 is ~~{aliened}~~ **[aligned]** with the projection lens 35. When a laser beam 37 is projected from the laser beam device toward the mask 33, the laser beam 37 becomes incident ~~{along}~~ **[on]** the mask ~~{pattern}~~. The laser beam incident to the mask 33 passes through

the projection lens 35 and is concentrated on ~~{a}~~ **[the]** substrate 31 ~~{having}~~**[, which has]** an amorphous silicon layer ~~{formed thereon, whereby polycrystallization}~~**[. Polycrystallization]** of the amorphous silicon layer is performed according to the mask pattern.

At this point, a growth of the polycrystalline grain is controlled by ~~{a}~~ **[the]** shape and ~~{an}~~ energy density of the laser beam**[,]** and ~~{a}~~ **[by the]** temperature and ~~{a}~~ cooling ~~{speed}~~ **[rate]** of the substrate. ~~{A}~~ **[During crystallization, a]** silicon grain ~~{during a crystallization process is divided into}~~ **[has]** three regions: a low energy density region; an intermediate energy density region; and a high energy density region. The low energy density region is a partially ~~{melt}~~ **[melted]** region. That is, the lower energy density region is one **[in]** which ~~{only a}~~ **[the]** lower portion of the silicon layer is not ~~{melt}~~ **[melted,]** and ~~{a}~~ **[thus the]** silicon melting depth is ~~{smaller}~~ **[less]** than ~~{a}~~ **[the]** thickness of the silicon layer ~~{and a}~~**[. The resulting]** grain diameter is ~~{smaller}~~ **[less]** than ~~{a}~~ **[the]** thickness of the silicon layer because seeds on the lower portion of the silicon layer **[tend to]** grow vertically.

The intermediate energy density region is an almost completely ~~{melt}~~ **[melted]** region. That is, the intermediate energy density is one which only ~~{part}~~ **[some]** of seeds on the lower portion of the silicon layer ~~{is}~~ **[are]** not completely melted. Except for ~~{part of seed on the lower portion of the silicon layer, almost part}~~ **[those seeds, almost all]** of the silicon layer is completely melted. This region is ~~{also}~~ a region ~~{that a}~~ **[in which]** lateral growth ~~{is possible centering}~~**[, centered]** on the seeds**[, is possible]**.

The high energy density region is one ~~{that}~~ **[in which]** even the ~~{lower}~~ **[lowest]** portion of the silicon layer is completely melted.

A crystallization method using the polycrystalline silicon crystallization equipment of Fig. 2 is as follows. The laser beam 37 is uniformed by predetermined means. Thereafter, ~~{a type of a}~~ **[the]** laser beam that will be formed on the substrate 31 is determined ~~{through}~~ **[by]** the mask 33. A laser beam having a width of tens of μ~~{b}~~ **[m]** is formed through the projection lens 35. The substrate 31 **[is]** arranged on a stage **[that]** moves slowly**[, usually]** at a speed of less than ~~{1 i/pulse,}~~ **[1μm /pulse,]** so that ~~{a}~~ crystallization is performed by the laser beam. The mask 33 has divided **[stripe shape]** regions "A", "B", and "C"~~{in shape of stripe}~~.

Fig. 3 is a plan view illustrating a mechanism ~~{that the amorphous silicon layer is crystallized through the laser beam. At this time, in first and second crystallization steps 45, a}~~ **[for laser crystallization of amorphous silicon. In a first crystallization step, shown in element 45,]**lateral growth occurs by moving the substrate 31. ~~{At}~~ **[In]** the second ~~{step, }~~**[crystallization step, also shown in element 45,]** a grain boundary 41 ~~{of}~~ **[formed in]** the first step moves and forms a new grain boundary ~~{41a.Preferably}~~ **[41a. Preferably]**, a high energy density ~~{for complete melting}~~ **[that completely melts the silicon]** is used, and ~~{a}~~ **[the]** width of the laser beam is ~~{smaller}~~ **[less]** than twice ~~{of}~~ the maximum lateral growth distance.

[The step and melt process continues.] After an n-th crystallization step, grains **[43]** of the polycrystalline silicon that ~~{is}~~ **[were]** crystallized by the lateral growth ~~{grows as}~~ **[are]** large ~~{as a grain 43}~~**[,]** and the grain boundary 41n is finally determined.

Fig. 4 is an enlarged view illustrating a portion D of Fig. 3. As shown in Fig. 4, the polycrystalline silicon layer has a protruding portion 45 that protrudes upwardly ~~{due to a later growth of the adjacent grains and}~~**[. The protruding portion]** is formed

on the grain boundary~~{. This is because the}~~ **[due to growth of adjacent grains. This result comes about because]**solid silicon is greater in volume than ~~{the}~~ liquid silicon, and the silicon layer melted **[last]** is ~~{lastly}~~ cooled at the grain boundary region, increasing ~~{a}~~ **[its]** volume. The protruding portion 45 has a height of about 300 Å.

Further, when the silicon layer is crystallized using the conventional crystallization described above, as shown in Fig. 5, defects 51, **[each]** referred to as a low angle defect, may exist on the surface of the layer. This ~~{is}~~ **[result comes about]** because the heat energy contained in the silicon layer is suddenly exhausted via the substrate below the silicon layer when the laser beam is blocked.

The defects on the surface of the silicon layer result from ~~{the}~~ sudden cooling, leading to ~~{an}~~ abnormal **[grain]** growth ~~{of the grains. }~~**[.]**

~~{The}~~ **[A]** polycrystalline silicon layer manufactured by the above-described method is **[usually]** patterned ~~{for}~~ **[to form]** a channel ~~{of the semiconductor layer}~~ in subsequent ~~{process, and then}~~ **[processes. Then,]** an insulating layer is formed on the polycrystalline silicon layer. In other words, since the insulating layer is formed on a non-flat surface ~~{of the semiconductor layer}~~ due to **[grain]** defects ~~{in the gains}~~ and the grain boundary ~~{protruded}~~ **[protruding]** upwardly, a trap level may occur due to a mismatch between the polycrystalline silicon layer and the insulating layer. ~~{Therefore,}~~ **[The result is that the]** field effect mobility of charges that flow along a surface of the polycrystalline silicon layer is significantly lowered, leading to ~~{a}~~ low reliability.

SUMMARY OF THE INVENTION

To overcome the problems described above, preferred embodiments of the

present invention provide a method of forming a polycrystalline silicon layer having excellent electrical characteristics.

In order to achieve the above object, the preferred embodiments of the present invention provide a method of forming a polycrystalline silicon layer, comprising: forming an amorphous silicon layer on a substrate~~{; a first step of}~~**[,]** melting ~~{completely}~~ the amorphous silicon layer ~~{using a laser beam thereby forming}~~ **[by passing a laser beam through a mask so as to form a polycrystalline silicon layer; and re-melting an upper portion of]** the polycrystalline silicon layer by ~~{adopting a mask; and a second step of melting an upper portion the polycrystalline silicon layer using the laser beam by adopting the mask thereby recrystallizing}~~ **[passing a laser beam through a mask so as to recrystallize]** the upper portion of the polycrystalline silicon layer.

The mask ~~{has}~~ **[used for crystallization causes the formation of]** a completely ~~{melting}~~ **[melted]** region and a partially ~~{melting}~~ **[melted]** region~~{. The}~~**[, wherein the]** completely ~~{melting}~~ **[melted]** region and the partially ~~{melting}~~ **[melted]** region have stripe shapes. The completely ~~{melting}~~ **[melted]** region and the partially ~~{melting}~~ **[melted]** region are postioned in series. The ~~{completely melting region}~~ **[portion]** of the mask ~~{pattern}~~ **[that causes a completely melted region]** is made of a material having a high light transmittance, and the ~~{partially melting region}~~ **[portion]** of the mask ~~{pattern}~~ **[that causes a partially melted region]** is made of a material having a low light transmittance. ~~{The first and second steps are proceeded through one}~~ **[Crystallization is beneficially performed using a]** scanning process of moving the substrate having the amorphous silicon layer under the laser beam.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

Figs. 1A to ~~{1C}~~ **[1B]** are plan views illustrating a typical crystallization process of a polycrystalline silicon layer;

Fig. 2 is a schematic perspective view illustrating a configuration of a polycrystalline silicon crystallization equipment using the ~~{eximer}~~ **[excimer]** laser annealing technique;

Fig. 3 is a plan view illustrating a mechanism ~~{that}~~ **[of crystallizing]** an amorphous silicon layer ~~{is crystallized through}~~ **[using]** the polycrystalline silicon crystallization equipment of Fig. 2;

Fig. 4 is an enlarged side view of "D" portion of Fig. 3;

Fig. 5 is a detailed plan view illustrating a surface of a polycrystalline silicon layer formed according to a conventional method;

Fig. 6 is a plan view illustrating a **[laser beam]** mask pattern ~~{for the laser beam}~~ according to an embodiment of the invention;

Fig. 7 is a plan view illustrating a crystallization process according to the embodiment of the invention; and

Fig. 8 is a cross-sectional view illustrating a polycrystalline silicon layer formed by ~~{a method of}~~ the embodiment of the invention compared to that formed by a conventional method.

DETAILED DESCRIPTION OF ~~{PREFFERED EMBODIMENTS}~~ [A PREFERRED EMBODIMENT]

Reference will now be made in detail to a preferred embodiment of the present invention, **[an]** example of which is illustrated in the accompanying drawings.

The forming method for a thin film transistor is follows. First, a gate electrode and a gate line (not shown) are formed on a substrate (not shown). Thereafter, an insulating layer of SiNx or SiO_2 is formed over the whole surface of the substrate. An amorphous silicon layer is **[then]** deposited on the insulating layer. ~~{In case that}~~ **[If]** the amorphous silicon layer is made of hydrogenized amorphous silicon, a dehydrogenation process is performed to remove hydrogen ~~{in advance}~~ before ~~{a}~~ crystallization ~~{process. It}~~**[. This]** is because pores, which may ~~{lower}~~ **[reduce the]** electrical characteristics of the polycrystalline silicon layer, may be formed while hydrogen is removed during ~~{the}~~ crystallization ~~{process. }~~**[.]**

~~{Sequentially, the}~~ **[The]** amorphous silicon layer is **[then]** crystallized using the mask pattern 109 shown in Fig. 6 ~~{and undertakes a lateral}~~**[. Lateral]** growth ~~{to form}~~ **[forms]** the polycrystalline silicon layer. ~~{At this point, the}~~ **[The]** mask pattern 109 includes a **[sequence of]** partially melting ~~{region}~~ **[regions]** 111 and ~~{a}~~ completely melting ~~{region}~~ **[regions]** 113 ~~{in series}~~. On the partially melting ~~{region}~~ **[regions]** 111~~{,}~~ a coating film having a low light transmittance is formed~~{, while the}~~**[. The]** completely melting region 113 has ~~{a}~~ good light transmittance. Therefore, ~~{the}~~ **[a]** laser ~~{beams}~~ **[beam]** that pass through the partially melting ~~{region}~~ **[regions]** 111 and the completely melting ~~{region 113 become}~~ **[regions 113 becomes beams having]** different ~~{in}~~ energy ~~{intensity}~~ **[intensities]**. The partially melting ~~{region 111 is a region that corresponds to the}~~ **[regions 111 correspond to a]**

low density energy region ~~{which}~~ **[that]** melts the silicon layer less than its full depth~~{, whereupon}~~**[. The result is that]** only an upper portion of the polycrystalline silicon layer ~~{can be melted. On the other hands, the}~~ **[is melted by the partially melting regions 111. The]** completely melting ~~{region 113 is a region that corresponds}~~ **[regions 113 correspond]** to the high energy density ~~{region. The}~~ **[regions. A]** laser beam that passes through ~~{the}~~ **[a]** completely melting region 113 has a width of about ~~{2 w}~~ **[2μm]** and completely melts the amorphous silicon layer~~{, so}~~ **[such]** that ~~{a later}~~ **[lateral]** growth can be sequentially performed. The completely melting ~~{region}~~ **[regions]** 113 and the partially melting ~~{region}~~ **[regions]** 111 have ~~{a}~~ stripe ~~{shape}~~ **[shapes]**. The completely melting region 113 advances the partially melting region with respect to the scanning direction.

Hereinafter, a method of forming ~~{the}~~ **[a]** polycrystalline silicon layer having a flat surface according to the preferred embodiment of the present invention is explained with reference to Fig. 7. As shown in Fig. 7, during a first laser annealing process, the laser beam scans ~~{the}~~ **[an]** amorphous silicon layer deposited on ~~{the}~~ **[a]** substrate 211 using the mask pattern 109. Portions 113a, 113b and 113c of the silicon layer are completely melted by the laser beam via the completely melting region 113, and other portions 111a, 111b and 111c of the silicon layer are partially melted by the laser beam via the partially melting region 111 of the mask pattern 109 (Fig. 6).

Subsequently, by moving the substrate 211, the polycrystalline silicon layer that is formed by the completely melting region 113 of the mask pattern 109 is scanned by the laser beam that passes through the partially melting region ~~{113}~~ **[111]** of the mask pattern 109, so that upper portions of the firstly completely melted portions 113a, 113b and 113c of the polycrystalline silicon layer is ~~{recyrstallized}~~ **[re-crystallized]**

up to a predetermined depth. Therefore, ~~{the}~~ **[a]** polycrystalline silicon layer having grains ~~{of}~~ **[with]** no ~~{defect}~~ **[defects]** and a flat surface can be manufactured. By moving the substrate sequentially, the complete melted portions 113a, 113b and 113c are fully ~~{recrystallized}~~ **[re-crystallized]** by the laser beam via the partially melting region 111 of the mask pattern 109. That is, the partial melting is sequentially performed at the same time, and the crystallization process is completed at an nth laser annealing process. The scanning process is completed when all the completely melted portions are over scanned by the laser beam via the partially melting ~~{region}~~ **[regions]** of the mask pattern 109.

Fig. 8 is a cross-sectional view illustrating a portion of ~~{the}~~ **[a]** polycrystalline silicon layer ~~{according to the preferred embodiment}~~ **[fabricated using the principles]** of the present invention. As shown in Fig. 8, the polycrystalline silicon layer formed through the first laser annealing process has a protruding portion "F" formed on the grain boundary region ~~{that the}~~ **[where]** adjacent grain boundaries contact ~~{with}~~ each other. The protruding portion "F" is melted and ~~{recrystallized through the second laser annealing process, so}~~ **[re-crystallized by the partially melting process such]** that the polycrystalline silicon layer becomes flatted. Then, using the method described above, the polycrystalline silicon layer having ~~{a}~~ **[the]** flat surface is patterned into the semiconductor layer in the form of an island. Then, source and drain electrodes (not shown) spaced apart from each other are formed to overlap both end portions of the semiconductor layer. Therefore, ~~{the}~~ **[a]** switching element according to the preferred embodiment is completely manufactured. In the preferred embodiment of the present invention, an inverted staggered TFT is exemplary explained, but the polycrystalline silicon layer **[also]** can be employed in a top gate type TFT.

As described ~~{herein}~~ before, **[by]** using the method of forming ~~{the}~~ **[a]** polycrystalline silicon layer according to the preferred embodiment of the present invention, defects in the grains can be removed~~{,}~~ and ~~{also the}~~ **[a]** protruding portion formed on ~~{the}~~ grain boundary ~~{region becomes flatted.}~~ **[regions can be flattened.]** Therefore, ~~{the}~~ **[a]** switching element having excellent electrical characteristics can be obtained.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.